



3A6000

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V1.2

2024 07

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3A6000

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3A6000

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4- 1			13
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4- 5			14
4- 6	w		14
4- 7	-		15
4- 8	w		15
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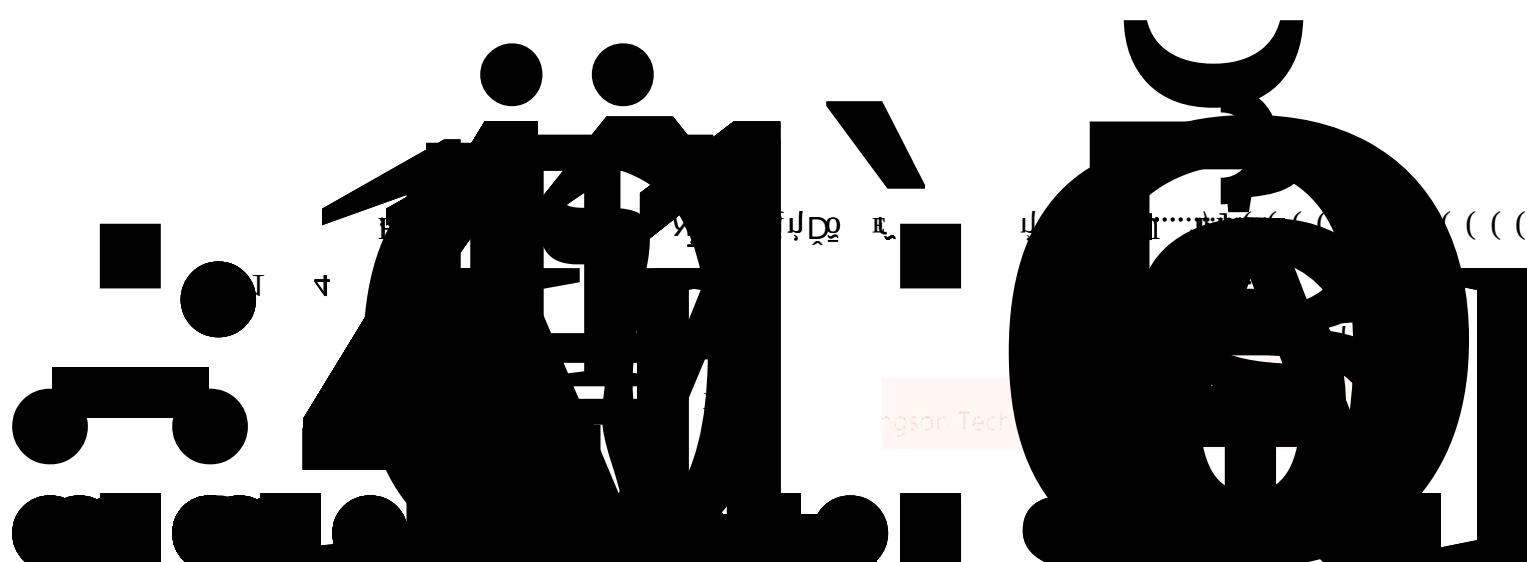
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14-	101	seqid	L		140
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1

1.1

$$0 \quad \quad \quad \downarrow \quad \quad \quad 1^\infty \quad \quad \quad \downarrow \quad \quad \quad 32 \quad \quad \quad \downarrow$$

3A6000

Y

S0 1 S2 S3 Master/Slave o M i

S SM/SS WM/WS NM/NS

X2 Master o " Cache e o

p L Slave o i r Yconf

X1 X2



3A6000

Y

5x5 i r " Cache i

IO o IO-RING

5x3 i r 4 " Cache DDR4 p L

i IO o IO-RING

IO-RING' o ' HT L MISC SE i r HT

L p DMA L DMA L IO DMA L

Ω No 128

i r 4

scache 256 p scache



2

2.1

3A6000 4 8

2.2

L DO_TEST CHIP_CONFIG[9:0]

2- 1 L



```
DO_TEST      1 ' b1    w
              1 ' b0
              ]
```

CHIP_CONFIG[9:4]



3

3°	↓	No	~	
0	1		48	4
~ No	16	✓	No 44	
3A6000	7	✓	44	✗ No

3.1

3A6000 1 4 8



4'h3	13:12	4'hb	29:28
4'h4	15:14	4'hc	31:30
4'h5	17:16	4'hd	33:32
4'h6	19:18	4'he	35:34
4'h7	21:20	4'hf	37:36

3A6000 44 No MC

interleave IOCSR[0x400] =

3- 3 44 No

addr[43:40]==4'hc	,uncache	SE
addr[43:40]==4'he	,uncache	HT
0x10000000-0x1fffffff, 0x3ff00000-0x3fff0fff()	,uncache	MISC
Mc interleave 0	,uncache	MC0
Mc interleave 1	,uncache	MC1
Scache interleave 0(scid_sel =)	,cache	Scache0
Scache interleave 1(scid_sel =)	,cache	Scache1
Scache interleave 2(scid_sel =)	,cache	Scache2
Scache interleave 3(scid_sel =)	,cache	Scache3

3.2

3A6000 IO-RING ~

Master [Master 8 ~

8 BASE MASK MMAP 64

BASE K MASK 1 MMAP

Slave ~ MMAP[4] MMAP[5] MMAP[6]

MMAP[7] ~

3- 4 MMAP

[7]	[6]	[5]	[4]
~	SCACHE/ 4		~

~ : (IN_ADDR & MASK) == BASE

3~



SCACHE/ SCID_SEL = 4 SCACHE 4
interleave_bit = 2 MC
0x1FE0_0000 IOCSR

3- 5

0x2000	CORE0_WIN0_BASE	0x2100	CORE1_WIN0_BASE
0x2008	CORE0_WIN1_BASE	0x2108	CORE1_WIN1_BASE
0x2010	CORE0_WIN2_BASE	0x2110	CORE1_WIN2_BASE
0x2018	CORE0_WIN3_BASE	0x2118	CORE1_WIN3_BASE
0x2020	CORE0_WIN4_BASE	0x2120	CORE1_WIN4_BASE
0x2028	CORE0_WIN5_BASE	0x2128	CORE1_WIN5_BASE
0x2030	CORE0_WIN6_BASE	0x2130	CORE1_WIN6_BASE
0x2038	CORE0_WIN7_BASE	0x2138	CORE1_WIN7_BASE
0x2040	CORE0_WIN0_MASK		



0x2238	CORE2_WIN7_BASE	0x2338	CORE3_WIN7_BASE
0x2240	CORE2_WIN0_MASK	0x2340	CORE3_WIN0_MASK
0x2248	CORE2_WIN1_MASK	0x2348	CORE3_WIN1_MASK
0x2250	CORE2_WIN2_MASK	0x2350	CORE3_WIN2_MASK
0x2258	CORE2_WIN3_MASK	0x2358	CORE3_WIN3_MASK
0x2260	CORE2_WIN4_MASK	0x2360	CORE3_WIN4_MASK
0x2268	CORE2_WIN5_MASK	0x2368	CORE3_WIN5_MASK
0x2270	CORE2_WIN6_MASK	0x2370	CORE3_WIN6_MASK
0x2278	CORE2_WIN7_MASK	0x2378	CORE3_WIN7_MASK
0x2280	CORE2_WIN0_MMAP	0x2380	CORE3_WIN0_MMAP
0x2288	CORE2_WIN1_MMAP	0x2388	CORE3_WIN1_MMAP
0x2290	CORE2_WIN2_MMAP	0x2390	CORE3_WIN2_MMAP
0x2298	CORE2_WIN3_MMAP	0x2398	CORE3_WIN3_MMAP
0x22a0	CORE2_WIN4_MMAP	0x23a0	CORE3_WIN4_MMAP
0x22a8	CORE2_WIN5_MMAP	0x23a8	CORE3_WIN5_MMAP
0x22b0	CORE2_WIN6_MMAP	0x23b0	CORE3_WIN6_MMAP
0x22b8	CORE2_WIN7_MMAP	0x23b8	CORE3_WIN7_MMAP
0x2400	SCACHE0_WIN0_BASE	0x2500	SCACHE1_WIN0_BASE
0x2408	SCACHE0_WIN1_BASE	0x2508	SCACHE1_WIN1_BASE
0x2410	SCACHE0_WIN2_BASE	0x2510	SCACHE1_WIN2_BASE
0x2418	SCACHE0_WIN3_BASE	0x2518	SCACHE1_WIN3_BASE
0x2420	SCACHE0_WIN4_BASE	0x2520	SCACHE1_WIN4_BASE
0x2428	SCACHE0_WIN5_BASE	0x2528	SCACHE1_WIN5_BASE
0x2430	SCACHE0_WIN6_BASE	0x2530	SCACHE1_WIN6_BASE
0x2438	SCACHE0_WIN7_BASE	0x2538	SCACHE1_WIN7_BASE
0x2440	SCACHE0_WIN0_MASK	0x2540	SCACHE1_WIN0_MASK
0x2448	SCACHE0_WIN1_MASK	0x2548	SCACHE1_WIN1_MASK
0x2450	SCACHE0_WIN2_MASK	0x2550	SCACHE1_WIN2_MASK
0x2458	SCACHE0_WIN3_MASK	0x2558	SCACHE1_WIN3_MASK
0x2460	SCACHE0_WIN4_MASK	0x2560	SCACHE1_WIN4_MASK
0x2468	SCACHE0_WIN5_MASK	0x2568	SCACHE1_WIN5_MASK
0x2470	SCACHE0_WIN6_MASK	0x2570	SCACHE1_WIN6_MASK
0x2478	SCACHE0_WIN7_MASK	0x2578	SCACHE1_WIN7_MASK
0x2480	SCACHE0_WIN0_MMAP	0x2580	SCACHE1_WIN0_MMAP
0x2488	SCACHE0_WIN1_MMAP	0x2588	SCACHE1_WIN1_MMAP
0x2490	SCACHE0_WIN2_MMAP	0x2590	SCACHE1_WIN2_MMAP
0x2498	SCACHE0_WIN3_MMAP	0x2598	SCACHE1_WIN3_MMAP
0x24a0	SCACHE0_WIN4_MMAP	0x25a0	SCACHE1_WIN4_MMAP
0x24a8	SCACHE0_WIN5_MMAP	0x25a8	SCACHE1_WIN5_MMAP
0x24b0	SCACHE0_WIN6_MMAP	0x25b0	SCACHE1_WIN6_MMAP

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-	-	0x2970	IO_L2X_WIN6_MASK
-	-	0x2978	IO_L2X_WIN7_MASK
-	-	0x2980	IO_L2X_WIN0_MMAP
-	-	0x2988	IO_L2X_WIN1_MMAP
-	-	0x2990	IO_L2X_WIN2_MMAP
-	-		

[7]	[6]	[5]	[4]
0	DDR interleaved		0
interleave_bit	IOCSR[0x0400]		0
	10		

7	DVFS_v1	R	1	1	
8	Tsensor	R	1	1	
9		R	1		
10		R	1		
11	Guest Mode	R	1		
12	Freq_scale_16	R	1	16 No	
13	Int Remap	R	1 ' b1	1	L
14	SE enabled	R	1 ' b0	1	SE w

4.3 0x0010

0x0010

4- 4

63:0	Vendor	R	0x6e6f7367_6e6f6f4c	“ Loongson ”
------	--------	---	---------------------	--------------

4.4 0x0020

0x0020

4- 5

63:0	ID	R	0x00003030_30364133	“ 3A6000 ”
------	----	---	---------------------	------------

4.5 0x0180



10	MC1_default_confspace	RW	1 ' b1	p
11		RW	1 ' b1	
12	MC1_resetrn	RW	1 ' b1	MC1
13	MC1_clken		1 ' b1	MC1
26:24	HT_freq_scale_ctrl	RW	3 ' b011	HT L Ne
27	HT_clken	RW	1 ' b1	HT
30:28				
31				
42:40	Node_freq_ctrl	RW	3 ' b111	Ne
43	-	RW	1 ' b1	
63:56	Cpu_version	R	2 ' h3F	CPU

4.6

0x0188

0x0188

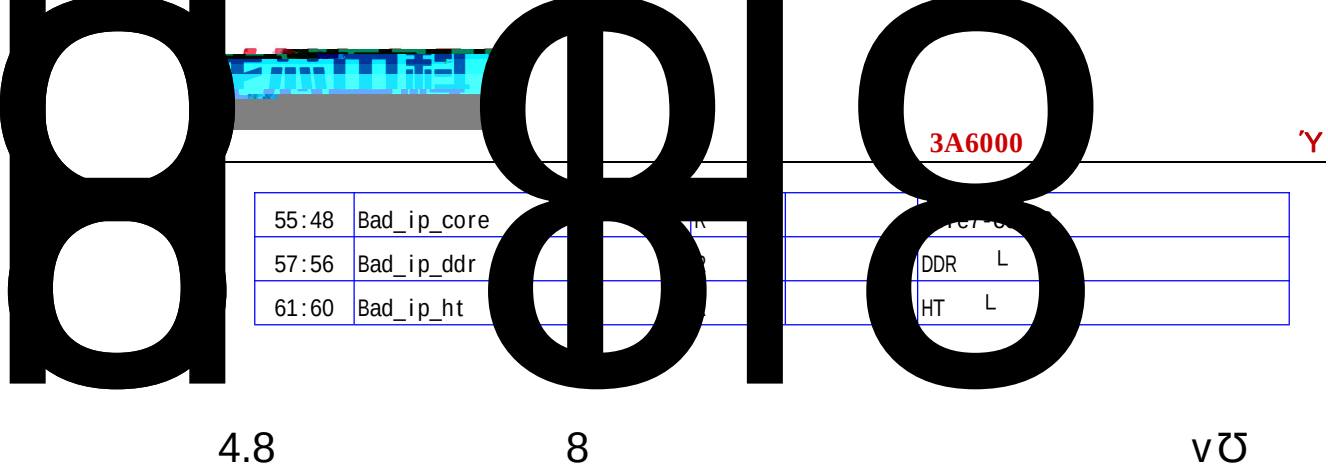
4- 7

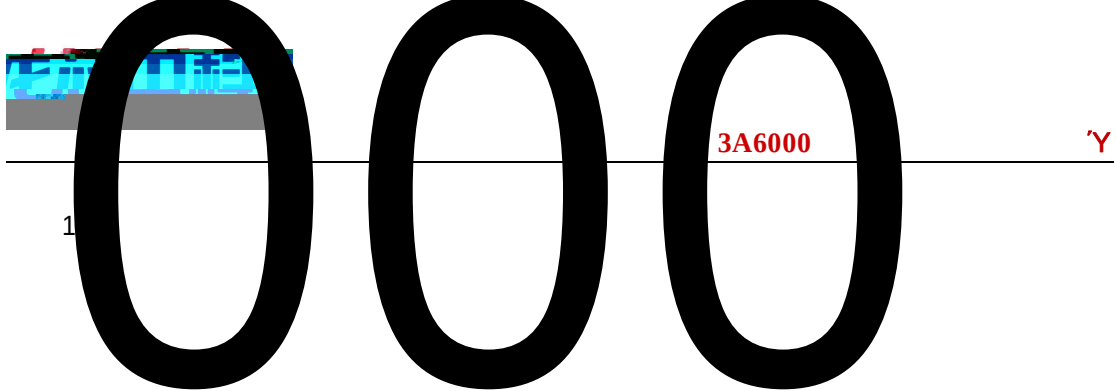
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15:0

19:16	HT sideband	RW	4 ' b0	HT L ~
23:20	I2C	RW	4 ' b0	I2C ~
27:24	UART	RW	4 ' b0	UART ~
31:28	SPI	RW	4 ' b1	SPI ~
35:32	GPIO	RW	4 ' b0	GPIO ~
39:36	SE UART	RW	4 ' b0	SE UART ~
43:40	SE SPI	RW	4 ' b0	SE SPI ~
47:44	SE I2C	RW	4 ' b0	SE I2C ~
51:48	î4j0			







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3A6000

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6		RW		
6		RW		L2 N Ne
		RW		3 ' b000
75:73	L2_FBDLY	RW		3 ' b000
79:76	L2_ICPSEL	RW		4 ' b0111
83:80	L2_FVCO_TUNE_ABS	RW		4 ' b0011
84	L2_SSC_SPRD	RW		0
85	L2_SSC_EN	RW		L2
95:86	-	RW		
115:96	L2_FRAC	RW		L2 Ne
119:116				
122:120	VDDA_LDO_CTRL	RW		
123	VDDA_LDO_BYPASS	RW		
126:124	VDDD_LDO_CTRL	RW		
127:124	VDDD_LDO_BYPASS	RW		
i	-	RW		

PLL ouput = clk_r



				NODE	NODE_CLOCK_SEL	1
				MEM PLL	MEM PLL	
[23:14]	MEM_PLL_DIV_LOOPC	RW	0x41	MEM PLL	MEM PLL	
[29:24]	MEM_PLL_DIV_OUT	RW	0x0	MEM PLL	MEM PLL	
[30]	NODE_CLOCK_SEL	RW	0x0	0	MEM_PLL	MEM
[31]	-			1	NODE_CLOCK	L2 PLL
[34:32]	VDDA_LDO_CTRL	RW				
[35]	VDDA_LDO_BYPASS	RW				
[38:36]	VDDD_LDO_CTRL	RW				
[39]	VDDD_LDO_BYPASS	RW				
[40]						



3A6000

'Y

11	core2_en	RW	0x1	2	1
14:12	core3_freqctrl	RW	0x7	3 No	L
15	core3_en	RW	0x1	3	
				:	No
				No	L +1 /8



12		RW	0x0	
14	Scahe_1MB	RW	0x0	Scache 1
19:16		RW	0x0	
24		RW	0x0	
31:30	mc_en	RW	0x3	MC 3 p



63:0	sram_ctrl	RW	0x0	p Sram
------	-----------	----	-----	--------

4.16 FUSE0 0x0460

No Fuse0 0x0460

4- 19 FUSE

127:0	Fuse_0	RW	0x0	
-------	--------	----	-----	--

4.17 FUSE1 0x0470

No Fuse1 0x0470

4- 20 FUSE

127:0	Fuse_1	RW	0x0	
-------	--------	----	-----	--



5

3A6000~ 1 ă SYS_CLOCK 4 ~

SYS_CLOCK No≠

3A6000 3 2 HT L 3 LA132 No≠ No

L

4 0x1fe00000 ~

IOCSR 4 0

~ [17:16] 4 0 ~

5.1

ă SYS_CLOCK 100MHz ~ 25MHz

CHIP_CONFIG[4]

HT PHY ă SYS CLOCK ~ PHY 200MHz No ă

CHIP_CONFIG[8] SYS CLOCK ă 25MHz

HT PHY 3.2GHz

3A6000 3 2 L

5- 1 0

			No	L	L
Boot Clock	SYS_CLOCK	*1			SPI UART I2C AVS L
	SYS PLL				SYS PLL 4
					Node Clock Core Clock HTcore
Main Clock	Back PLL	PLL			Clock LA132 Clock
					Mem Clock Stable Clock~
					~
Node Clock	Main Clock	*1			HT L
Core0 Clock	Main Clock	*1			Core0
Core1 Clock	Main Clock	*1			Core1
Core2 Clock	Main Clock	*1			Core2
Core3 Clock	Main Clock	*1			Core3
HTcore Clock	Node Clock	*1			HT L No



3A6000

Y

Mem Clock	MEM PLL	PLL			ρ L
	Back PLL	/2 /4 /8			ρ L

5.2

No

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j

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M



5- 3 ĩ w

35:32	freqscale_mode_core	RW	0x0	0: (n+1)/8 1: 1/(n+1)

5.2.2

3A6000

No

No

L /

No

L

7

“ ĩ w ”

L

0x1fe00000

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 4201 GORDON AVENUE
 ARLINGTON, VA 22204-4302

5.3.1

5- 6 w

5- 7 ì w

5.3.2

$\bar{U}$ No

No $\bar{U}$

$\tilde{\alpha}$ 1212.3



5.4 HT

HT L No L i w i
0x1fe00000 ~ IOCSR 0x0180

5- 8 w

26:24	HT_freq_scale_ctrl	RW	3 ' b111	HT L No	
27	HT_clken	RW	1 ' b1	HT	

i No L HT L ~ No



3A6000

Y

GPIO_FUNC_en[13] 1 stable counter GPIO[13] L
GPIO 0x1fe00000 IOCSR
0x0500

5- 11 GPIO

0





7 GPIO

3A6000 20 GPIO No i w
GPIO w i
0x1fe00000

7.1 0x0500

0x1fe00000 0x0500
7- 1

31:0	GPIO_OEn	RW	32 'hfffffff	GPIO
63:32	GPIO_FUNC_En	RW	32 'hfff0000	GPIO w

7.2 0x0508

0x1fe00000 0x0508
7- 2





7.4 GPIO



7.5 GPIO

3A6000 GPIO ~

GPIO00 GPIO008 GPIO016 " L 0~

GPIO001 GPIO009 GPIO017 " L 1~

GPIO002 GPIO010 GPIO018 " L 2~

GPIO003 GPIO011 GPIO019 " L 3~

GPIO004 GPIO012 " L 4~

GPIO005 GPIO013 " L 5~

GPIO006 GPIO014 " L 6~

GPIO007 GPIO015 " L 7~

GPIO020-GPIO31

GPIO GPIO_INT_en L GPIO_INT_POL L

0x1fe00000

0x0510

7- 5 L

31:0	GPIO_INT_POL	RW	32 ' h0	GPIO 0 - 1 -
63:32	GPIO_INT_en	RW	32 ' h0	GPIO L

L 7 i GPIO ~ ü

POL 0 1 1 ü L



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17:15 LLFTP_ver		1	Δ	3 ' h1
21	LSPW	1	1	1 ' b1
22	LAM	1	AM* 1	1 ' b1
0	CCDMA	1	Cache Coherent DMA	1 ' b1
1	SFB	1	Store Fill Buffer SFB	1 ' b1
3	LLEXC	1	LL 0 V w	1 ' b1
4	SCDLY	1	SC w	1 ' b1
5	LLDBAR	1	LL - dbar w	1 ' b1
0x3	6	1	ITLB TLB	1 ' b1
	7	1	ICache	1 ' b1
10:8 SPW_LVL		1	page walk	3 ' h4
11	SPW_HP_HF	1	page walk TLB	1 ' b1
12	RVA	1	w	1 ' b1
16:13	RVMAX-1	1	-1	4 ' h7
0x4	31:0	CC_FREQ	1 Hz	N/A
	15:0	CC_MUL		N/A
0x5	31:16	CC_DIV	No	N/A
	0	PMP	1	1 ' b1
0x6	3:1	PMVER	1 Δ	3 ' h1
	7:4	PMNUM	-1	4 ' h3
	13:8	PMBITS	-1	6 ' h3f
0x10	14	UPM	1 0	1 ' b1
	0	L1 IU_Present	1	Cache Cache 1 ' b1
	1	L1 IU Unify	1	L1 IU_Present Cache 1 ' b0
	2	L1 D Present	1	Cache 1 ' b1
	3	L2 IU Present	1	Cache Cache 1 ' b1
	4	L2 IU Unify	1	L2 IU_Present Cache 1
	5	L2 IU Private	1	L2 IU_Present Cache 1
	6	L2 IU Inclusive	1	L2 IU_Present Cache 1



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'Y

		L1			
7	L2 D Present	1	Cache		1 ' b0
8	L2 D Private	1	Cache	i	



8.2 3A6000

3A6000	IOCSR				
IOCSR		ρ	JTAG	η	
IOCSR	IOCSR RD.B/H/W/D	IOCSRWR.B/H/W/D	Ω	ι	
IOCSR RD.B/H/W/D	IOCSR RD.B/H/W/D rd, rj		ι	rj	
IOCSR	IOCSR	ρ	Ω	rd	IOCSRWR.B/H/W/D
IOCSRWR.B/H/W/D rd, rj	W/ ι	rj		IOCSR	
rd	Ω	IOCSR	IOCSR RD.B/H/W/D	jd,	D7
IOCSR RD.B/H/W/ D	jd,	D	~	l	psâ ¢\$ R

9 Cache SCache

SCache

3A6



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Slock2_mask	0x0250	[47:0]	2~	o
Slock3_valid	0x0218	[63:63]	3~	o
Slock3_addr	0x0218			



	en			
36	MCC clean shared replace en	RW	1 ' b0	



10

3A6000 8 IPI BIOS
3A6000 3
No#

10.1

3A6000 ↓ 0x1fe00000
IOCSR 0x3ff00000
disable_0x3ff0 L 10- 1 | 10- 5
3A6000 8 3
8 7/8 No 4 7 0x1fe10000
[17:16] 0 3
10- 1 10- 1 w

	Ω				
IPI_Status	R	32	1		INT4
IPI_Enable	RW	32	L		
IPI_Set	W	32	Ω 1	↑	STATUS 1
IPI_Clear	W	32	Ω 1	↑	STATUS 0
MailBox0	RW		α	64 32	uncache
MailBox01	RW		α	64 32	uncache
MailBox02	RW		α	64 32	uncache
MailBox03	RW		α	64 32	uncache

3A6000 10- 1 w

10- 2 0

Core0_IPI_Status	0x1000	R	0	IPI_Status
Core0_IPI_Enable	0x1004	RW	0	IPI_Enable



Core0_IPI_Set	0x1008	W	0~	IPI_Set
Core0_IPI_Clear	0x100c	W	0~	IPI_Clear
Core0_MailBox0	0x1020	RW	0~	IPI_MailBox0
Core0_MailBox1	0x1028	RW	0~	IPI_MailBox1
Core0_MailBox2	0x1030	RW	0~	IPI_MailBox2
Core0_MailBox3	0x1038	RW	0~	IPI_MailBox3

10- 3 1~



Core1_IPI_Status	0x1100	R	1~	IPI_Status
Core1_IPI_Enalbe	0x1104	RW	1~	IPI_Enalbe
Core1_IPI_Set	0x1108	W	1~	IPI_Set
Core1_IPI_Clear	0x110c	W	1~	IPI_Clear
Core1_MailBox0	0x1120	R	1~	IPI_MailBox0
Core1_MailBox1	0x1128	RW	1~	IPI_MailBox1
Core1_MailBox2	0x1130	W	1~	IPI_MailBox2
Core1_MailBox3	0x1138	W	1~	IPI_MailBox3

10- 4 2~



Core2_IPI_Status	0x1200	R	2~	IPI_Status
Core2_IPI_Enalbe	0x1204	RW	2~	IPI_Enalbe
Core2_IPI_Set	0x1208	W	2~	IPI_Set
Core2_IPI_Clear	0x120c	W	2~	IPI_Clear
Core2_MailBox0	0x1220	R	2~	IPI_MailBox0
Core2_MailBox1	0x1228	RW	2~	IPI_MailBox1
Core2_MailBox2	0x1230	W	2~	IPI_MailBox2
Core2_MailBox3	0x1238	W	2~	IPI_MailBox3

10- 5 3~



Core3_IPI_Status	0x1300	R	3~	IPI_Status
Core3_IPI_Enalbe	0x1304	RW	3~	IPI_Enalbe
Core3_IPI_Set	0x1308	W	3~	IPI_Set
Core3_IPI_Clear	0x130c	W	3~	IPI_Clear
Core3_MailBox0	0x1320	R	3~	IPI_MailBox0
Core3_MailBox1	0x1328	RW	3~	IPI_MailBox1
Core3_MailBox2	0x1330	W	3~	IPI_MailBox2
Core3_MailBox3	0x1338	W	3~	IPI_MailBox3



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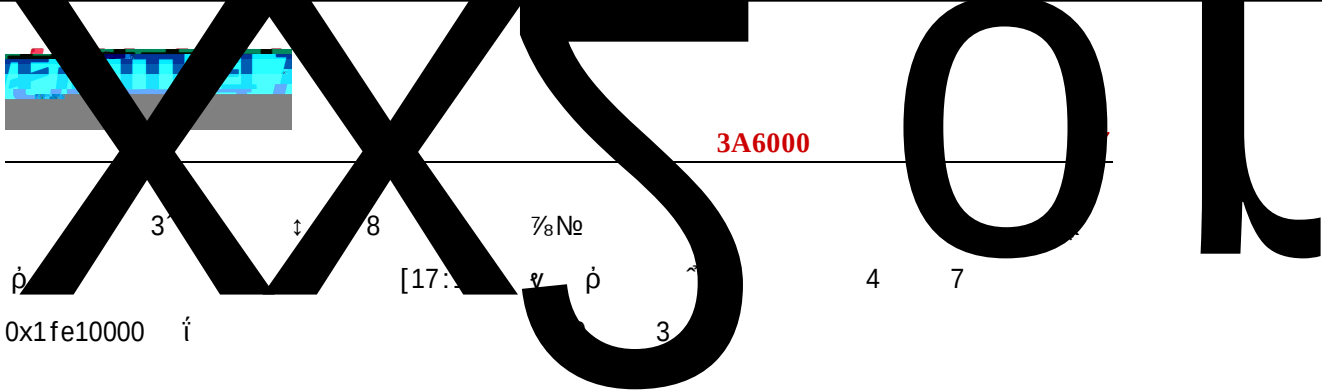
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8





10.2

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10- 6

		s L€	
perCore_IPI_Status	0x1000	R	IPI_Status
perCore_IPI_Enalbe	0x1004	RW	IPI_Enalbe
perCore_IPI_Set	0x1008	W	IPI_Set
perCore_IPI_Clear	0x100c	W	IPI_Clear
perCore_Mai lBox0	0x1020	RW	IPI_Mai lBox0
perCore_ MailBox1	0x1028	RW	IPI_Mai lBox1
perCore_ MailBox2	0x1030	RW	IPI_Mai lBox2
perCore_ MailBox3	0x1038	RW	IPI_Mai lBox3

MailBox

beço 6





			0 - MailBox0 32 1 - MailBox0 32 2 - MailBox1 32 3 - MailBox1 32 4 - MailBox2 32 5 - MailBox2 32 6 - MailBox3 32 7 - MailBox4 32 [1:0]
FREQ_Send	0x1058	WO	32 [31] 1 [30:27] Ω mask 32 Ω Ω 1000b Ω 0-2 0000b † 0-3 Ω [26] [25:16] ~ [15:5] [4:0] Ω IOCSR[0x1050]
Mail_Send			7 ~ 0 32 0 64
No 0	Mail_Box p		i
0 Mail_Box 0			

10.3

A †

7 Ω

⌘ ⌘ [IPI_Send Mail_Send Freq_Send Any_Send ~
i

10- 8

ANY_Send	0x1158	WO	64 [63:32] Ω [31] 1 [30:27] Ω mask 32 Ω Ω 1000b Ω 0-2 0000b † 0-3 Ω [26]
----------	--------	----	--



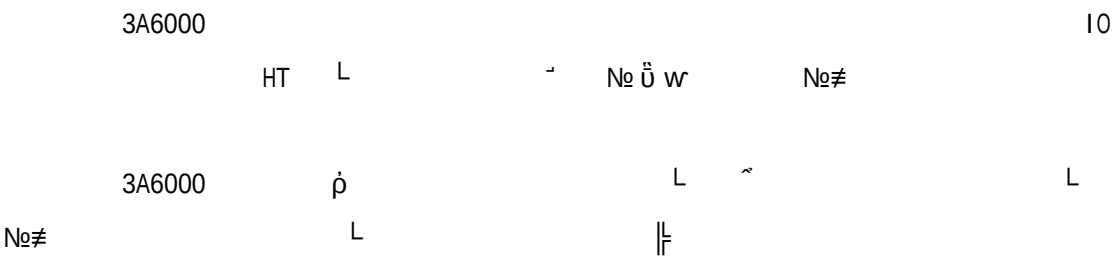
3A6000

Y

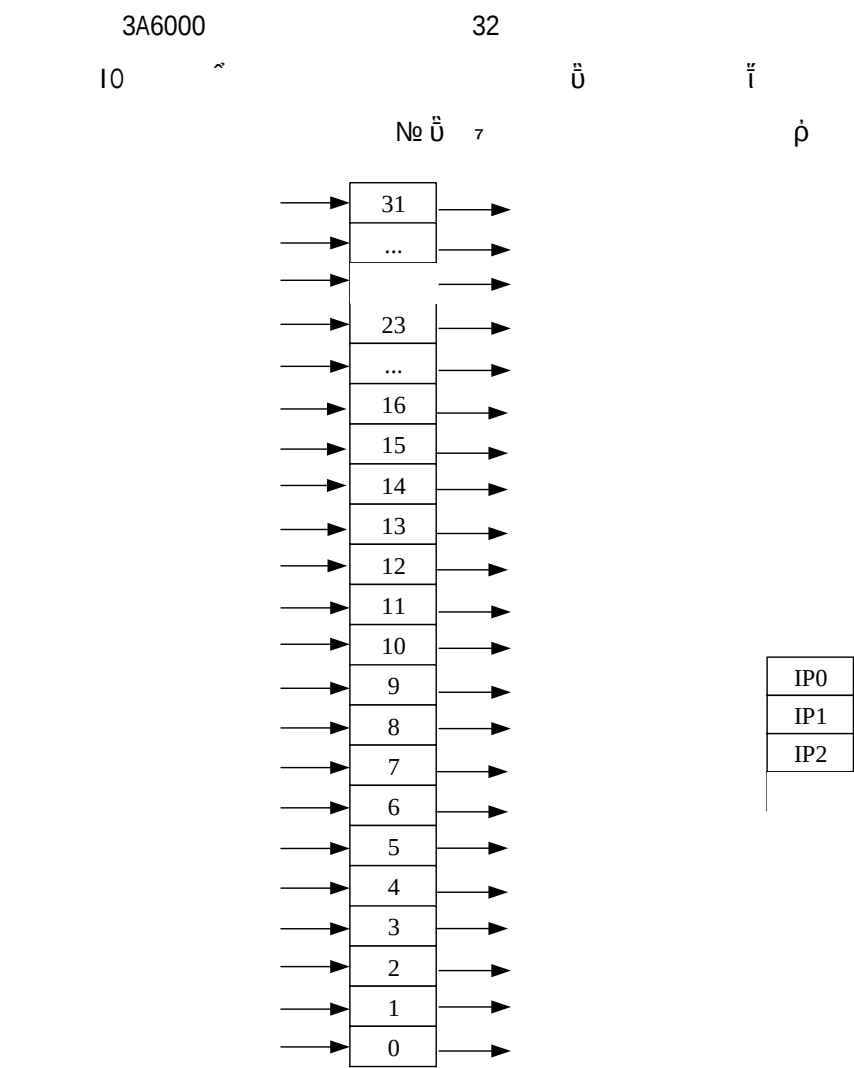
			[25:16] ~
			[15:0] Ω



11 I/O



11.1 I/O



11- 1 L

/					
	Intedge	Inten	Intenset	Intenclr	
0	RW / 0	R / 0	RW / 0	RW / 0	GPIO24/16/8/0/SC0
1	RW / 0	R / 0	RW / 0	RW / 0	GPIO25/17/9/1/SC1
2	RW / 0	R / 0	RW / 0	RW / 0	GPIO26/18/10/2/SC2
3	RW / 0	R / 0	RW / 0	RW / 0	GPIO27/19/11/3/SC3
4	RW / 0	R / 0	RW / 0	RW / 0	GPIO28/20/12/4
5	RW / 0	R / 0	RW / 0	RW / 0	GPIO29/21/13/5
6	RW / 0	R / 0	RW / 0	RW / 0	GPIO30/22/14/6
7	RW / 0	R / 0	RW / 0	RW / 0	GPIO31/23/15/7
8	RW / 0	R / 0	RW / 0	RW / 0	GPIO32/24/16/8/SC0



11- 4

Entry0	0x1400	GPI024/16/8/0	Entry16	0x1410	
Entry1	0x1401	GPI025/17/9/1	Entry17	0x1411	
Entry2	0x1402	GPI026/18/10/2	Entry18	0x1412	
Entry3	0x1403	GPI027/19/11/3	Entry19	0x1413	
Entry4	0x1404	GPI028/20/12/4	Entry20	0x1414	
Entry5	0x1405	GPI029/21/13/5	Entry21	0x1415	
Entry6	0x1406	GPI030/22/14/6	Entry22	0x1416	
Entry7	0x1407	GPI031/23/15/7	Entry23	0x1417	
Entry8	0x1408	I2C0	Entry24	0x1418	HT1-int0
Entry9	0x1409	I2C1	Entry25	0x1419	HT1-int1
Entry10	0x140a	UART0	Entry26	0x141a	HT1-int2
Entry11	0x140b	MCO	Entry27	0x141b	HT1-int3
Entry12	0x140c	MC1/AVS	Entry28	0x141c	HT1-int4
Entry13	0x140d	SPI	Entry29	0x141d	HT1-int5
Entry14	0x140e	Thsens	Entry30	0x141e	HT1-int6
Entry15	0x140f	UART1	Entry31	0x141f	HT1-int7

11.1.2

3A6000



11- 5

perCore_INTISR	0x1010	32

11.2 I/O

IO

3A6000

I/O

HT

256

No 0

Y

P

HT

0

1 IO



IO 11- 6
0x1fe00000 IOCSR 0x0420

48	EXT_INT_en	RW	0x0	IO
IO	HT	0	1	No 0
256				

11.2.1

IO 11- 7
0x1fe00000 3A6000
8 3 8
7/8 No 17:16
v p 4 7 0x1fe10000 i
0 3

EXT_IOIen[63:0]	0x1600	IO	[63:0]
EXT_IOIen[127:64]	0x1608	IO	[127:64]
EXT_IOIen[191:128]			



3A6000

Y

11- 10 Y



EXT_I0Imap3	0x14C3	EXT_I0I [127:96]
EXT_I0Imap4	0x14C4	EXT_I0I [159:128]
EXT_I0Imap5	0x14C5	EXT_I0I [191:160]
EXT_I0Imap6	0x14C6	EXT_I0I [223:192]
EXT_I0Imap7	0x14C7	EXT_I0I [255:224]

11- 14 3 8 L i 11- 13
 11- 14 i [7:4] 11- 15
 0x48 [EXT_I0I_node_type4 3~

11- 13

3:0	~
7:4	11- 15

No 0 EXT_I0Ibounce 1 ~
 ~ EXT_I0Ibounce ~
 11- 13 0x27 11- 15 EXT_I0I_node_type2
 0x0013 No 0 0 0 1 0 2
 1 0 1 1 1 2 4 0 4 1 4 2
 No 0 EXT_I0Ibounce 0 ~ bitmap 7
 1 0 0

11- 14

EXT_I0Imap_Core0	0x1C00	EXT_I0I [0]
EXT_I0Imap_Core1	0x1C01	EXT_I0I [1]
EXT_I0Imap_Core2	0x1C02	EXT_I0I [2]
EXT_I0Imap_Core254	0x1CFE	EXT_I0I [254]
EXT_I0Imap_Core255	0x1CFF	EXT_I0I [255]

11- 15

EXT_I0I_node_type0	0x14A0	16 0
EXT_I0I_node_type1	0x14A2	16 1
EXT_I0I_node_type2	0x14A4	16 2



EXT_I0I_node_type15	0x14BE	1615

11.2.2

7 0 7 1 15

11- 16 IO

perCore_EXT_I0Isr[63:0]	0x1800	IO [63:0]
perCore_EXT_I0Isr[127:64]	0x1808	IO [127:64]
perCore_EXT_I0Isr[191:128]	0x1810	IO [191:128]
perCore_EXT_I0Isr[255:192]	0x1818	IO [255:192]

11.2.3 IO

IO No 0 v IO 0
IO ~ ≠

11- 17 IO 0

EXT_I0I_send	0x1140	WO	IO [7:0]
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11.2.4 IO HT

HT HT HT L p HT
256 'P 256 No 4 8 'P 7
HT IO
7 1 3 p No 0 7 4
8 1 No 0
IO HT HT L 0 L



3A6000

12

12.1

3A6000 p
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~

g
0x1fe00198 g
w L

a



3A6000

24

L 1
|| 3A6000 ρ 2
~ 0 1
4 L
L 0 3
i i 0

L
No

12- 3

L

Thsen x1460

RW



[7:7]	Scale_sel0	0
[8:8]	Scale_sel0	0
[11:10]	Scale_sel0	0
[14:12]	Scale_freq0	No
[23:16]	Scale_gate1	1
[24:24]	Scale_en1	1
[27:26]	Scale_sel1	1
[30:28]	Scale_freq1	No
[39:32]	Scale_gate2	2
[40:40]	Scale_en2	2
[43:42]	Scale_sel2	2
[46:44]	Scale_freq2	No
[55:48]		

L
Thsens_freq_scale 0x1480 RW



3A6000

Y

PROCHOTn

PROCH

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THERMTRIPn

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12- 5

L

L			
	[0:0]	prochotn_oe PROCHOTn	Ť L 0 Ť
	1		
	[5:4]	prochotn_o_sel PROCHOTn	Ť
	[10:8]	prochotn_freq_scale PROCHOTn	Nŉ
0x1498	RW	[17:16]	thermtripn_o_sel THERMTRIPn Ť

12.5

3A6000 Ŗ

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1

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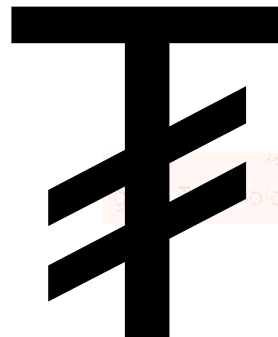
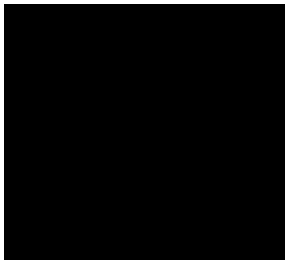
0x1FE00000

~

IOCSR

0x01580+vtensor_id<<4,

0x01588+vtensor_id<<4 è





11:9	Temp_cluster	RW	0	Thsens_trigger

12- 7

3	Out_mode	R	0	0 1 1
6:4	Out_cluster	R	0	
7	Overflow	R	0	
29:16	Data	R	0	

✂

$$= \text{data} * 820 / 0x4000 - 311 \quad -40 \sim 125$$
$$1 = (\text{data} + 110) * 1.226 / 0x1000$$

13 DDR4 SDRAM

3A6000 ρ ρ L DDR4 SDRAM % JESD79-4

13.1 DDR4 SDRAM

13.2 DDR4 SDRAM

13.2.1

13- 1 ρ L $\approx$ $\ddot{\alpha}$ $\downarrow$

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
PHY								



Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0					
0x0000						version(RD)							
0x0008						switch_byte48	x4_mode	ddr3_mode	capability RD				
0x0010											dram_init(RD)	init_start	
0x0018													
0x0020						preamble2		rdfifo_valid					
0x0028						rdfifo_empty(RD)					Overflow(RD)		
0x0030	dll_value(RD)		dll_init_done(RD)	dll_lock_mode	dll_bypass	dll_adj_cnt	dll_increment	dll_start_point					
0x0038	dll_dbl_fix					dll_close_disable		dll_ck					
0x0040						clken_ckca							
0x0048													
0x0050													
0x0058						clken_ds_0							
0x0060						clken_ds_1							
0x0068													
0x0070													
0x0078													



3A6000

Y

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x0110	rdodt_ctrl_0	rdgate_len_0	rdgate_mode_0	rdgate_ctrl_0			dqs_oe_ctrl_0	dq_oe_ctrl_0
0x0118				odt_len_add_0		dly_2x_0	redge_sel_0	rddqs_phase_0(RD)
0x0120	w_bdlly0_0[31:28]	w_bdlly0_0[27:24]	w_bdlly0_0[23:20]	w_bdlly0_0[19:16]	w_bdlly0_0[15:12]	w_bdlly0_0[11:8]	w_bdlly0_0[7:4]	w_bdlly0_0[3:0]
0x0128		w_bdlly0_0[59:56]	w_bdlly0_0[55:52]	w_bdlly0_0[51:48]	w_bdlly0_0[47:44]	w_bdlly0_0[43:40]	w_bdlly0_0[39:36]	w_bdlly0_0[35:32]
0x0130	w_bdlly1_0[24:21]	w_bdlly1_0[20:18]	w_bdlly1_0[17:15]	w_bdlly1_0[14:12]	w_bdlly1_0[11:9]	w_bdlly1_0[8:6]	w_bdlly1_0[5:3]	w_bdlly1_0[2:0]
0x0138								w_bdlly1_0[27:26]
0x0140							rg_bdlly_0[7:4]	rg_bdlly_0[3:0]
0x0148								
0x0150	rdqsp_bdlly_0[31:28]	rdqsp_bdlly_0[27:24]	rdqsp_bdlly_0[23:20]	rdqsp_bdlly_0[19:16]	rdqsp_bdlly_0[15:12]	rdqsp_bdlly_0[11:8]	rdqsp_bdlly_0[7:4]	rdqsp_bdlly_0[3:0]
0x0158								rdqsp_bdlly_0[35:32]
0x0160	rdqsn_bdlly_0[31:28]	rdqsn_bdlly_0[27:24]	rdqsn_bdlly_0[23:20]	rdqsn_bdlly_0[19:16]	rdqsn_bdlly_0[15:12]	rdqsn_bdlly_0[11:8]	rdqsn_bdlly_0[7:4]	rdqsn_bdlly_0[3:0]
0x0168								rdqsn_bdlly_0[35:32]
0x0170	rdq_bdlly_0[24:21]	rdq_bdlly_0[20:18]	rdq_bdlly_0[17:15]	rdq_bdlly_0[14:12]	rdq_bdlly_0[11:9]	rdq_bdlly_0[8:6]	rdq_bdlly_0[5:3]	rdq_bdlly_0[2:0]
0x0178								rdq_bdlly_0[27:26]
0x0180					dll_1xdly_1	dll_1xgen_1	dll_wrds_1	dll_wrds_1
0x0188		vref_sample_1	vref_clk_inv_1	dll_vref_1	vref_dly_1	dll_gate_1	dll_rddqs_1	dll_rddqs_0_1
0x0190	rdodt_ctrl_1	rdgate_len_1	rdgate_mode_1	rdgate_ctrl_1			dqs_oe_ctrl_1	dq_oe_ctrl_1
0x0198				odt_len_add_1		dly_2x_1	redge_sel_1	rddqs_phase_1(RD)
0x01a0	w_bdlly0_1[31:28]	w_bdlly0_1[27:24]	w_bdlly0_1[23:20]	w_bdlly0_1[19:16]	w_bdlly0_1[15:12]	w_bdlly0_1[11:8]	w_bdlly0_1[7:4]	w_bdlly0_1[3:0]
0x01a8		w_bdlly0_1[59:56]	w_bdlly0_1[55:52]	w_bdlly0_1[51:48]	w_bdlly0_1[47:44]	w_bdlly0_1[43:40]	w_bdlly0_1[39:36]	w_bdlly0_1[35:32]
0x01b0	w_bdlly1_1[24:21]	w_bdlly1_1[20:18]	w_bdlly1_1[17:15]	w_bdlly1_1[14:12]	w_bdlly1_1[11:9]	w_bdlly1_1[8:6]	w_bdlly1_1[5:3]	w_bdlly1_1[2:0]
0x01b8								w_bdlly1_1[27:26]
0x01c0							rg_bdlly_1[7:4]	rg_bdlly_1[3:0]
0x01c8								
0x01d0	rdqsp_bdlly_1[31:28]	rdqsp_bdlly_1[27:24]	rdqsp_bdlly_1[23:20]	rdqsp_bdlly_1[19:16]	rdqsp_bdlly_1[15:12]	rdqsp_bdlly_1[11:8]	rdqsp_bdlly_1[7:4]	rdqsp_bdlly_1[3:0]
0x01d8								rdqsp_bdlly_1[35:32]
0x01e0	rdqsn_bdlly_1[31:28]	rdqsn_bdlly_1[27:24]	rdqsn_bdlly_1[23:20]	rdqsn_bdlly_1[19:16]	rdqsn_bdlly_1[15:12]	rdqsn_bdlly_1[11:8]	rdqsn_bdlly_1[7:4]	rdqsn_bdlly_1[3:0]
0x01e8								rdqsn_bdlly_1[35:32]
0x01f0	rdq_bdlly_1[24:21]	rdq_bdlly_1[20:18]	rdq_bdlly_1[17:15]	rdq_bdlly_1[14:12]	rdq_bdlly_1[11:9]	rdq_bdlly_1[8:6]	rdq_bdlly_1[5:3]	rdq_bdlly_1[2:0]
0x01f8								rdq_bdlly_1[27:26]
0x0200					dll_1xdly_2	dll_1xgen_2	dll_wrds_2	dll_wrds_2
0x0208		vref_sample_2	vref_clk_inv_2	dll_vref_2	vref_dly_2	dll_gate_2	dll_rddqs_2	dll_rddqs_0_2
0x0210	rdodt_ctrl_2	rdgate_len_2	rdgate_mode_2	rdgate_ctrl_2			dqs_oe_ctrl_2	dq_oe_ctrl_2



3A6000

Y

Offset



3A6000

'Y

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x0320	w_bdlly0_4[31:20]							



100-1 技术股份有限公司



	3:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
CTL								
0x1000	tMRD	tRP	tWLDQSEN	tMOD	tXPR		tCKE	tRESET
0x1008								tODTL
0x1010	tREFretention				tRFC		tREF	
0x1018	tCKESR	tXSRD	tXS		tRFC_dlr			tREF_IDLE
0x1020								



3A6000

Y

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:-K4
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Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x1260	retry_cnt(RD)					rbuffer_max(RD)	rdfifo_depth	stat_en
0x1268	pm_rdage_low		pm_rdage_up		pm_pref_near_full	pm_hot_en	pm_hot_minus	pm_hot_count
0x1270	pm_stb_error(R0)			pm_stb_deb_cnt_sel	pm_stb_dbg_cnt			
0x1278	pm_stb_adjust				pm_stb_distance	stb_context_gnt	pm_stb_cold_time	
0x1280	aw_512_align		rd_before_wr	ecc_enable		int_vector(RD)	int_trigger(RD)	int_enable
0x1288	pm_stb_arprior_cfg							
0x1290						i		



int





3A6000

Y

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x13d0	odt_rd_cs_map							



3A6000

Y

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
└ ┘								
0x1580	win0_mask							
0x1588	win1_mask							
0x1590	win2_mask							
0x1598	win3_mask							
0x15a0	win4_mask							
0x15a8	win5_mask							
0x15b0	win6_mask							
0x15b8	win7_mask							
└ ┘								
0x1600	win0_mmap							
0x1608	win1_mmap							
0x1610	win2_mmap							
0x1618	win3_mmap							
0x1620	win4_mmap							
0x1628	win5_mmap							
0x1630	win6_mmap							
0x1638	win7_mmap							
└ ┘								
0x1680	write_train_data[63:0]							
0x1688	write_train_data[127:64]							
0x1690	write_train_data[191:128]							
0x1698	write_train_data[255:192]							
0x16a0	write_train_data[319:256]							
0x16a8	write_train_data[383:320]							
0x16b0	write_train_data[447:384]							
0x16b8								



3A6000

Y

Offset



3A6000

Y

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x21a8	cs_turnaround(R0)							
0x21b0	bg_conflict(R0)							
└┐								
0x2300						sm_leveling	sm_init	
0x2308								
0x2310	sm_rank_03			sm_rank_02		sm_rank_01	sm_rank_00	
0x2318	sm_rank_07			sm_rank_06		sm_rank_05	sm_rank_04	
0x2320	sm_rank_11			sm_rank_10		sm_rank_09	sm_rank_08	
0x2328	sm_rank_15			sm_rank_14		sm_rank_13	sm_rank_12	
0x2330	sm_rank_19			sm_rank_18		sm_rank_17	sm_rank_16	
0x2338	sm_rank_23			sm_rank_22		sm_rank_21	sm_rank_20	
0x2340	sm_rank_27			sm_rank_26		sm_rank_25	sm_rank_24	
0x2348	sm_rank_31			sm_rank_30		sm_rank_29	sm_rank_28	
└┐								
0x2430	cache_monitor_cnt(R0)							
0x2438	cache_monitor_cnt(R0)							

0x5350



3A6000

Y

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x2638	fix_r2r_dly_count(R0)				fix_w2w_dly_count(R0)			
0x2640	fix_r2w_dly_count(R0)				fix_w2r_dly_count(R0)			
TST								
0x3000						lpbk_mode		



3A6000

Y

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x3178	obs[255:192] (R0)							
0x3180	obs[319:256] (R0)							
0x3188	obs[383:320] (R0)							
0x3190	obs[447:384] (R0)							
0x3198	obs[511:448] (R0)							
0x31a0	obs[575:512] (R0)							
0x31a8	obs[639:576] (R0)							
0x31b0	obs[671:640](R0)							
└ ┘								
0x3200								
0x3208								
0x3220	tud_i0							
0x3228	tud_i1							
0x3230	tud_o(R0)							
└ ┘								
0x3300	tst_300							
0x3308	tst_308							
0x3310	tst_310							
0x3318	tst_318							
0x3320	tst_320							
0x3328	tst_328							
0x3330	tst_330							
0x3338	tst_338							
0x3340	tst_340							
0x3348	tst_348							
0x3350	tst_350							
0x3358	tst_358							
0x3360	tst_360							
0x3368	tst_368							
0x3370	tst_370							
0x3378	tst_378							



13.3

13.3.1

Δ . Init_start 0x010 Ω 0x2 Init_start

~ || i

√ DRAM Δ .

(1) pm_clk_sel_ckca pm_clk_sel_ds

(2) pm_phy_init_start 1 Δ . PHY

(3) DLL √ pm_dll_init_done 1

(4) pm_dll_lock_* pm_pll_lock_* i 1

(5) pm_clken_*

(6) pm_init_start 1 p L Δ .

(7) p L Δ . √ pm_dram_init pm_cs_enable

13.3.2

STR v √ L ~ pad_reset_po 0x808

≠ DDR_RESETh L L

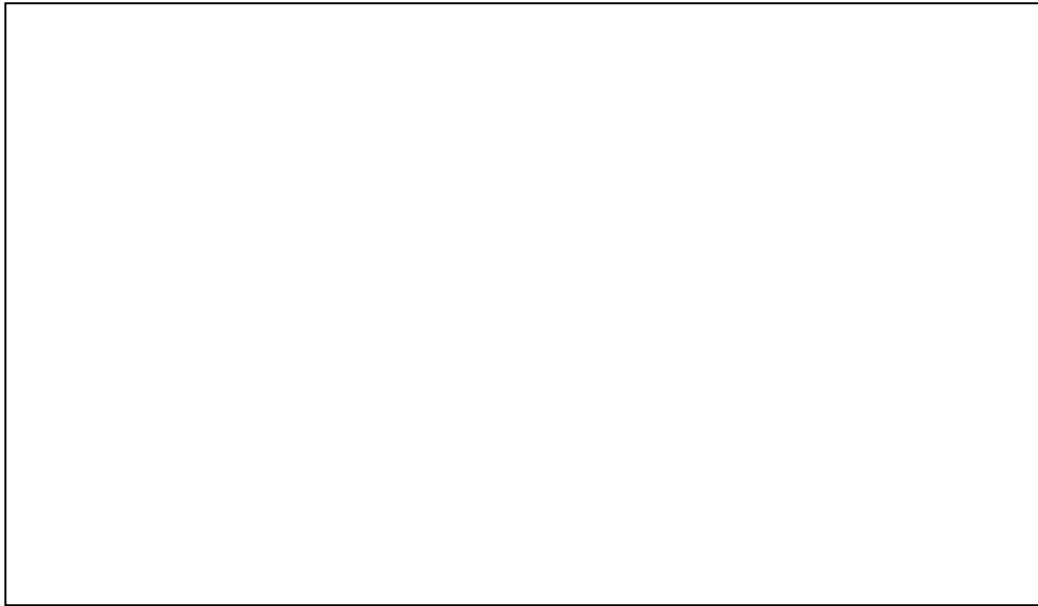
(1) reset_ctrl[1:0] == 2 ' b00 ~

L i DDR_RESETh p

L Δ .



(3) pm_pad_reset_o[1:0] == 2'b01
 DDR_RESETn



STR L 2
 STR 3
 1

13.3.3 Leveling

Leveling DDR4
 Write Leveling Read Leveling Gate Leveling
 Write Leveling Gate Leveling Read Leveling
 Read Leveling Leveling DQS
 GATE DQ DQ
 bit-deskew w dataslice bit



13.3.1 Write Leveling

Write Leveling	Ω DQS	τ	ǎ
(1) L Δ . ǎ	ρ		
(2) Dll_wrdqs_x x = 0 ÷ 8	0x20		
(3) Dll_wrdq_x x = 0 ÷ 8	0x0		
(4) Lvl_mode 2 ' b01			
(5) Lvl_ready	1	~	Write Leveling
(6) Lvl_req 1			
(7) Lvl_done	1		Write Leveling
(8) Lvl_resp_x	0	↑	Dll_wrdq_x[6:0]
dll_1xdly[6:0] v 1	5-7	Lvl_resp_x 1	9
1 ↑ Dll_wrdq_x[6:0]	dll_1xdly[6:0] v 1	5-7	
Lvl_resp_x 0	Dll_wrdq_x[6:0]	dll_1xdly[6:0]	
v 1	5-7	Lvl_resp_x 1	9
(9) Dll_wrdq_x dll_1xdly	∴ 0x40	Dll_wrdq_x	dll_1xdly
(10) DIMM pm_dly_2x	0x0	~	pm_dly_2x
v 0x010101			
(11) Lvl_mode 0x700	2 ' b00	≠	Write Leveling

13.3.3.2 Gate Leveling

Gate Leveling	L ρ	DQS o	ǎ
(1) L Δ . ǎ	ρ		
(2) Write Leveling ǎ	ρ		
(3) Dll_gate_x x = 0 ÷ 8	0		
(4) Lvl_mode 2 ' b10			
(5) Lvl_ready	1	~	Gate Leveling
(6) Lvl_req 1			
(7) Lvl_done	1		Gate Leveling -≠ M B



0 ↓

(4) Ω Mrs_req 0x1126 1 DRAM Ü MRS

(5) Mrs_done 0x1127 1 ↓ MRS Ü ~ ₪

0 ↓

(6)



(6) Lpbk_error 1 0 ~
Lpbk_* 7
0 7

13.3.8 ECC

ECC width 64 ~
Ecc_enable 1



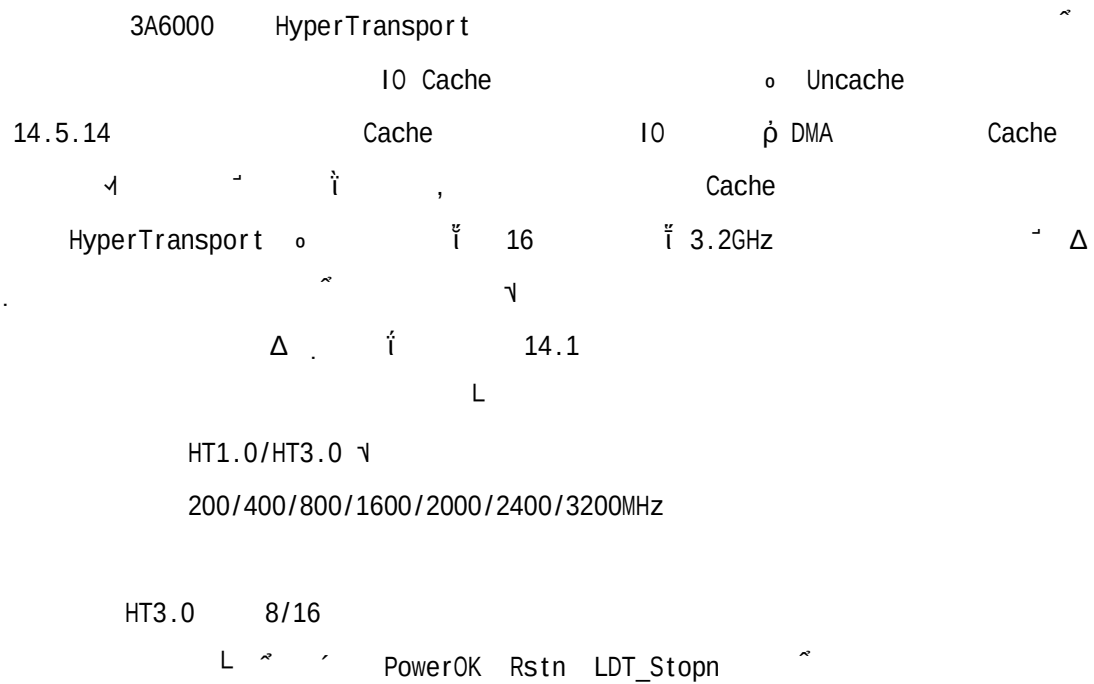
13- 3 1~ ρ L 𐄂

		L	
1~ ρ L ECC Mc1_ecc_set	0x0700	RW	1~ ρ L ECC [5:0]: MC1 int_enable [8]: MC1 int_trigger 0 [21:16]: MC1 int_vector(R0) 7 [33:32]: MC1 ecc_enable ECC 7 w [40]: MC1 rd_before_wr 0 w
	0x0708	RW	
1~ ρ L ECC Mc1_ecc_cnt	0x0710	RW	1~ ρ L ECC [7:0]: MC1 int_cnt ECC 0 [15:8]: MC1 int_cnt_err(R0) ECC 7 [23:16]: MC1 int_cnt_fatal(R0) ECC 7
1~ ρ L ECC 𐄂 Mc1_ecc_cs_cnt	0x0718	RO	1~ ρ L ECC 𐄂 [7:0]: MC1 ecc_cnt_cs_0 CS0 𐄂 ECC [15:8]: MC1 ecc_cnt_cs_1 CS1 𐄂 ECC [23:16]: MC1 ecc_cnt_cs_2 CS2 𐄂 ECC [31:24]: MC1 ecc_cnt_cs_3 CS3 𐄂 ECC [39:32]: MC1 ecc_cnt_cs_4 CS4 𐄂 ECC [47:40]: MC1 ecc_cnt_cs_5 CS5 𐄂 ECC [55:48]: MC1 ecc_cnt_cs_6 CS6 𐄂 ECC [63:56]: MC1 ecc_cnt_cs_7 CS7 𐄂 ECC
1~ ρ L ECC Mc1_ecc_code	0x0720	RO	1~ ρ L ECC [7:0]: MC1 ecc_code_64 64 ECC ECC ρ w [41:32]: MC1 ecc_code_256 256 ECC ECC ρ w [52:48]: MC1 ecc_code_dir ρ ECC 7 ρ w [60:56]: MC1 ecc_data_dir ρ ECC 7 ρ w
1~ ρ L ECC 𐄂 Mc1_ecc_code	0x0728	RO	1~ ρ L ECC 𐄂

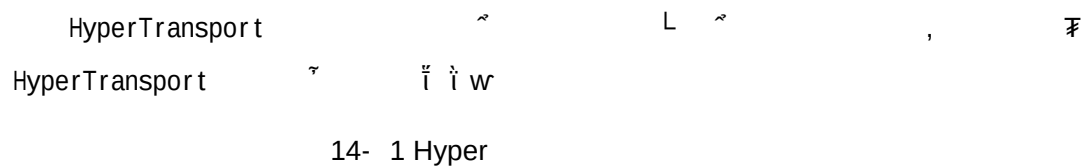


Mc1_ecc_addr			[63:0]: MC1_ecc_addr ECC 32
1~0 Mc1_ecc_data0	0x0730	RO	1~0 [63:0]:Mc1_ecc_data0 ECC 32 64 ECC 256 ECC [63:0]
1~1 Mc1_ecc_data1	0x0738	RO	1~1 [63:0]:Mc1_ecc_data1 ECC 32 256 ECC [127:64]
1~2 Mc1_ecc_data2	0x0740	RO	1~2 [63:0]:Mc1_ecc_data2 ECC 32 256 ECC [191:128]
1~3 Mc1_ecc_data3	0x0748	RO	1~3 [63:0]:Mc1_ecc_data3 ECC 32 256 ECC [255:192]

14 HyperTransport



14.1 HyperTransport





x01xxx	NPC or PC	Write	bit 5 0 - Nonposted 1 - Posted bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 Don't Care
01xxxx	NPC	Read	bit 3 Don't Care bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 Don't Care
110000	R	RdResponse	
110011	R	TgtDone	Ω
111010	PC	Broadcast	
111100	PC	FENCE	↖
111111	-	Sync/Error	Sync/Error

Ü

Ü

14- 3

Ü

			‰
000000	-	NOP	ˆ
x01x0x	NPC or PC	Write	bit 5 0 - Nonposted 1 - Posted bit 2 0 - Byte 1 - Doubleword bit 0 0
010x0x	NPC	Read	bit 2 0 - Byte 1 - Doubleword bit 0 Don't Care
110000	R	RdResponse	
110011	R	TgtDone	Ω
111111	-	Sync/Error	↖ Ü

14.3 HyperTransport

HyperTransport L 256 ~ Fix Arbiter
E0I L
Ω L
í L 14.514.5.7 L

14.3.1 PIC

L PIC v
ĩ PIC PIC L Ü PIC
PIC L Ü PIC L Ü PIC
L 7 4 PIC L Ü 3 PIC Ω
3A6000 HyperTransport L 3 PIC Ω



256 4 4
PIC L 0 7

14.3.2

HT L 0
HT L
3 CPU
HT
HT L 0xeffdfb000080
HT L

14.3.3

3A6000 IO
HT PIC
P
IO
0x1800
HT L
IO
HT L
HT L

4.4.1 HyperTransport 3.0
 3A6000 HyperTransport 3.0 6000

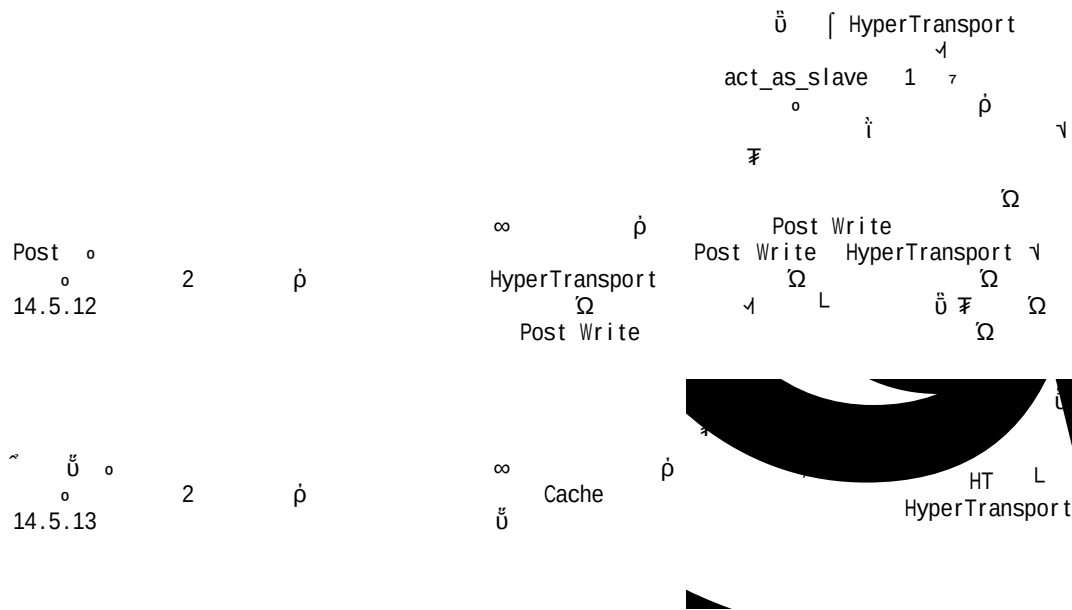
14- 5 HyperTransport 3.0

0x0E00_0000_0000	0x0EFF_FFFF_FFFF	1 TB	HT 3.0
------------------	------------------	------	--------

HyperTransport 3.0 33.2 HyperTransport 3.0 40

14- 6 3.0 HyperTransport 3.0 40

0x00_0000_0000	0xFC_FFFF_FFFF	1012 GB	MEM
0xFD_0000_0000	0xFD_0FFF_FFFF	256 MB	
0xFD_1000_0000	0xFD_F7FF_FFFF	3712 MB	
0xFD_F800_0000	0xFD_F8FF_FFFF	16 MB	
0xFD_F900_0000	0xFD_F90F_FFFF	1 MB	PIC
0xFD_F910_0000	0xFD_F91F_FFFF	1 MB	
0xFD_F920_0000	0xFD_FAFF_FFFF	30 MB	
0xFD_FB00_0000	0xFD_FBFF_FFFF	16 MB	HT 3.0
0xFD_FC00_0000	0xFD_FDFF_FFFF	32 MB	I/O
0xFD_FE00_0000	0xFD_FFFF_FFFF	32 MB	HT
0xFE_0000_0000	0xFF_FFFF_FFFF	8 GB	





	0x20				
	0x24				
	0x28	Cardbus CIS Pointer			
	0x2c	Subsystem ID		Subsystem Vendor ID	
	0x30	Expansion ROM Enable Address			
	0x34	Reserved			Capabilities Pointer
	0x38	Reserved			
	0x3c	Bridge Control		Interrupt Pin	Interrupt Line
Cap 0 PRI	0x40	Command		Capabilities Pointer	Capability ID
	0x44	Link Config 0		Link Control 0	
	0x48	Link Config 1		Link Control 1	
	0x4C	LinkFreqCap0		Link Error0/Link Freq 0	Revision ID
	0x50	LinkFreqCap1		Link Error1/Link Freq 1	Feature
	0x54	Error Handling		Enumeration Scratchpad	
	0x58	Reserved		Mem Limit Upper	Mem Enable Upper
Cap 1 Retry	0x60	Capability Type	Reserved	Capability Pointer	Capabiliter ID
	0x64	Status 1	Control 1	Status 0	Control 0
	0x68	Retry Count 1		Retry Count 0	
CAP 3	0x6C	Capability Type	Revision ID	Capability Pointer	Capabiliter ID
CAP 4 Interrupt	0x70	Capability Type	Index	Capability Pointer	Capabiliter ID
	0x74	Dataport			
	0x78	IntrInfo[31:0]			
	0x7C	IntrInfo[63:32]			
Int Vector	0x80	INT Vector[31:0]			
	0x84	INT Vector[63:32]			
	0x88	INT Vector[95:64]			
	0x8C	INT Vector[127:96]			
	0x90	INT Vector[159:128]			
	0x94	INT Vector[191:160]			



	0x98	INT Vector[223:192]			
	0x9C	INT Vector[255:224]			
	0xA0	INT Enable[31:0]			
	0xA4	INT Enable[63:32]			
	0xA8	INT Enable[95:64]			
	0xAC	INT Enable[127:96]			
	0xB0	INT Enable[159:128]			
	0xB4	INT Enable[191:160]			
	0xB8	INT Enable[223:192]			
	0xBC	INT Enable[255:224]			
CAP 5 Gen3	0xC0	Capability Type	Cap Enum/Index	Capability Pointer	Capabiliter ID
	0xC4	Global Link Training			
	0xC8	Transmitter Configuration 0			
	0xCC	Receiver Configuration 0			
	0xD0	Link Training 0			
	0xD4	Frequency Extension			
	0xD8	Transmitter Configuration 1			
	0xDC	Receiver Configuration 1			
	0xE0	Link Training 1			
	0xE4	BIST Control			

Enable	0x100	Device ID		Vendor ID	
	0x104	Status		Command	
	0x108	Class Code			Revision ID
	0x10c	BIST	Header Type	Latency Timer	Cache Line Size
	0x110				
	0x114				
	0x118				
	0x11c				
	0x120				
	0x124				
	0x128	Cardbus CIS Pointer			



	0x12c	Subsystem ID	Subsystem Vendor ID
	0x130	Expansion ROM Enable Address	
	0x134	Reserved	Capabilities Pointer
	0x138	Reserved	
	0x13c	Bridge Control	Interrupt Pin Interrupt Line
Receive Windows	0x140	HT RX Enable 0	
	0x144	HT RX Mask 0	
	0x148	HT RX Enable 1	
	0x14C	HT RX Mask 1	
	0x150	HT RX Enable 2	
	0x154	HT RX Mask 2	
	0x158	HT RX Enable 3	
	0x15C	HT RX Mask 3	
	0x160	HT RX Enable 4	
	0x164	HT RX Mask 4	
Header Trans	0x168	HT RX Header Trans	
	0x16C	HT RX EXT Header Trans	
Post Windows	0x170	HT TX Post Enable 0	
	0x174	HT TX Post Mask 0	
	0x178	HT TX Post Enable 1	
	0x17C	HT TX Post Mask 1	
Prefetchable Windows	0x180	HT TX Prefetchable Enable 0	
	0x184	HT TX Prefetchable Mask 0	
	0x188	HT TX Prefetchable Enable 1	
	0x18C	HT TX Prefetchable Mask 1	
Uncache Windows	0x190	HT RX Uncache Enable 0	
	0x194	HT RX Uncache Mask 0	
	0x198	HT RX Uncache Enable 1	
	0x19C	HT RX Uncache Mask 1	
	0x1A0	HT RX Uncache Enable 2	
	0x1A4	HT RX Uncache Mask 2	
	0x1A8	HT RX Uncache Enable 3	



	0x1AC	HT RX Uncache Mask	3
	0x1B0	HT RX P2P Enable	0
P2P	0x1B4	HT RX P2P Mask	0
Windows	0x1B8	HT RX P2P Enable	1
	0x1BC	HT RX P2P Mask	1
	0x1C0	APP Configuration	0
APP	0x1C4	APP Configuration	1
Config	0x1C8	RX Bus Value	
	0x1CC	PHY status	
	0x1D0	TX Buffer	0
Buffer	0x1D4	TX	



3A6000

Y

	0x26C	HT TX POST ID WIN3
INT TRANS WINDOW	0x270	INT TRANS WIN lo
	0x274	INT TRANS WIN hi

i

14.5.1 Bridge Control

0x3C

0x00000000

Bus Reset Control

14- 8 Bus Reset Control

31:23	Reserved	9	0x0		
22	Reset	1	0x0	R/W	L 0->1 HT_RSTn 0 1->0 HT_RSTn 1
21:0	Reserved	22	0x0		

14.5.2 Capability Registers

0x40

0x00006008

Command Capabilities Pointer Capability ID



3A6000

Y

	Pointer				
7:0	Capability ID	8	0x08	R	HyperTransport capability ID

0x44

0x00112000

Link Config Link Control

14- 10 Link Config Link Control



30:28 Link Width Out 3



3A6000

Y

7:0

Revision ID

8

0x60

R/W

~

3.0

3A6000



[0,4,8,12┆┆252] 0

[1,5,9,13┆┆253] 1

[2,6,10,14┆┆254] 2

[3,7,11,15┆┆255] 3

ht_int_stripe_1 3 ~ |

0x80

0x00000000

HT [31:0]

14- 20 HT 1

31:0	Interrupt_case [31:0]	32	0x0	R/W	HT [31:0]

0x84

0x00000000

HT [63:32]

14- 21 HT 2

31:0	Interrupt_case [63:32]	32	0x0	R/W	HT [63:32]

0x88

0x00000000

HT [95:64]

14- 22 HT 3

31:0	Interrupt_case [95:64]	32	0x0	R/W	HT [95:64]

0x8c

0x00000000

HT [127:96]

14- 23 HT 4

|--|--|



3A6000

Y

14.5.8

256 1 0
256 | i

14.5.7

0xa0

0x00000000

HT

[31:0]

14- 27 HT

1



31:0 Interrupt_mask 32 0x0 R/W H1
[31:0]



14- 30 HT

4

31:0	Interrupt_mask [127:96]	32	0x0	R/W	HT [127:96]

0xb0

0x00000000

HT [159:128]

14- 31 HT

5

31:0	Interrupt_mask [159:128]	32	0x0	R/W	HT [159:128]

0xb4

0x00000000

HT [191:160]

14- 32 HT

6

31:0	Interrupt_mask [191:160]	32	0x0	R/W	HT [191:160]



14.5.10

```
HT    L    o
hit = ( BASE & MASK ) == ( ADDR & MASK )
addr_out_trans  raddrOut    t
```



3A6000

Y

15:0	ht_rx_image0_mask[39:24]	16	0x0	R/W	HT	o 0	[39:24]
------	--------------------------	----	-----	-----	----	-----	---------

0x148

0x00000000

HT o 1

14- 38 HT o 1

31	ht_rx_image1_en	1	0x0	R/W	HT	o 1	~
30	ht_rx_image1_trans_en	1	0x0	R/W	HT	o 1	~
29	ht_rx_image1_multi_node_en	1	0x0	R/W	HT	o 1	

[39:37]



						[39:37] [46:44]	
28	ht_rx_image2_conf_hit_en	1	0x0	R/W	HT	0	2
25:0	ht_rx_image2_trans[49:24]	26	0x0	R/W	HT		[49:24]

0x154

0x00000000

HT 2

14- 41 HT 2

31:16	ht_rx_image2_base[39:24]	16	0x0	R/W	HT	0	[39:24]
15:0	ht_rx_image2_mask[39:24]	16	0x0	R/W	HT	0	[39:24]

0x158

0x00000000

HT 3

14- 42 HT 3

31	ht_rx_image3_en	1	0x0	R/W	HT	0	3
30	ht_rx_image3_trans_en	1	-				



31:16	ht_rx_image3_base[39:24]	16	0x0	R/W	HT	o 3	[39:24]
15:0	ht_rx_image3_mask[39:24]	16	0x0	R/W	HT	o 3	[39:24]

0x160

0x00000000

HT o 4

14- 44 HT o 4

31	ht_rx_image4_en	1	0x0	R/W	HT	o 4	~
30	ht_rx_image4_trans_en	1	0x0	R/W	HT	o 4	~
29	ht_rx_image4_multi_node_en	1	0x0	R/W	HT	o 4	[39:37] [46:44]
28	ht_rx_image4_conf_hit_en	1	0x0	R/W	HT	o 4	1 0
25:0	ht_rx_image4_trans[49:24]	26	0x0	R/W	HT	o 4	[49:24]

0x164

0x00000000

HT o 4

14- 45 HT o 4

31:16	ht_rx_image4_base[39:24]	16	0x0	R/W	HT	o 4	[39:24]
15:0	ht_rx_image4_mask[39:24]	16	0x0	R/W	HT	o 4	[39:24]

14.5.11

HT 1x

0x168

0x00000000

14- 46



3A6000

'Y



0xFD_FE000000

31	ht_rx_header_trans_ext	1	0x1	R/W	type1	24	28
EXT HEADER							

30	ht_rx_header_trans_en
----	-----------------------



3A6000

'Y



ACC o)

29:23



0x00000000

HT POST 0 2 p

14- 52 HT POST 0 2 p



31	ht_post2_en	1	0x0	R/W	HT	POST	0 2	~
30	ht_split2_en	1	0x0	R/W	HT	^	(	CPU uncache
					ACC	0)		
29:23	Reserved	14	0x0					
15:0	ht_post2_trans[39:24]							



14- 55 HT POST 0 3 0

31:16	ht_post3_base[39:24]	16	0x0	R/W	HT	POST	0 3	[39:24]
15:0	ht_post3_mask[39:24]	16	0x0	R/W	HT	POST	0 3	[39:24]

14.5.13

0

14.5.10

0

AXI

[

0

0

i CACHE

0

HT

i

0

CACHE

0

HT

4

↑

0x180

0x00000000

HT

~

0

0

0

14- 56 HT

~

0

0

0

31	ht_prefetch0_en	1	0x0	R/W	HT	~	0	~
30:16	Reserved	15	0x0					
15:0	ht_prefetch0_trans[39:24]	16	0x0	R/W	HT	~	0	[39:24]

0x184

0x00000000

HT

~

0

0

0

14- 57 HT

~

0

0

0



3A6000

Y

14- 58 HT ~ ů ° 1 ð



31 ht_prefetch1_en 1 0x0 R/W HT ~ ů etch



3A6000

'Y



28 ht_uncache0_conf_hit_en 1 0x0 R/W HT uncache o 0 1

25:0 ht_uncache0_trans[49:24] 26 0x0 R/W HT uncache o 0



3A6000

'Y

14- 63 HT

Uncache

o 1

ρ



31:16



3A6000

Y

31	ht_uncache3_en	1	0x0	R/W	HT	uncache	o 3	~
30	ht_uncache3_trans_en	1	0x0	R/W	HT			

3A6000

0 -> 1

LDT DISCONNECT HT

LDT_REQ_n

28	Ldt Req Gen	1	0x0	R/W	0 'P 1 0 -> 1 Ü ƒ Ω ~
27	rx sample en	1	0x0	R/W	cad cti 0x1c8
26	Dword Write	1	0x1	R/W	32/64/128/256 MEM

3A6000

					3A6000	Y
					111 0	
15	Int	1	0x0	R/W	CRC	0
14:12	Crc Int route	2	0	R/W	CRC	
11	Reserved					
10	ht int 8 bit	1	0x0	R/W	8	
					3	i
9:8	ht_int_stripe	2	0x0	R/W	0x0 ht_int_stripe_1	
					0x1 ht_int_stripe_2	
					0x2 ht_int_stripe_4	
					%o i	[
					SMI NMI INIT	
					INTTH,	
4:0	Interrupt Index	5	0x0	R/W		

14.5.18 PHY

PHY

0x1C00

0x83308000

PHY

14- 75 PHY

31:29	Reserved	3	0x0	R	
28	dll locked hi	1	0x0	R	8 DLL
27	dll locked lo	1	0x0	R	8 PLL
26	cdr locked hi	1	0x0	R	8 CDR
25	cdr locked lo	1	0x0	R	8 CDR
24	phase locked	1	0x0	R	
23:20	phy state	4			



14- 76 ũ

--	--	--	--	--	--	--

31:24	B_CMD_txbuffer	8	0x0	R	ũ	B
23:16	R_CMD_txbuffer	8	0x0	R	ũ	R
15:8	NPC_CMD_txbuffer	8	0x0	R	ũ	NPC , p



3A6000

Y

7:0	PC_DATA_txbuffer	8	0x0	R	0	PC
-----	------------------	---	-----	---	---	----

14.5.21

0 HT L 0 II M :

0

0x1D8

0x00000000

0

14- 78 0





3A6000

Y

0

7:4 NPC_CMD_txadj 4 0x0 R/W



14- 83 Training 2

31:0	T2 time	32	0x7fffff	R/W	Training 2

14.5.27 Training 3

HyperTransport 3.0

Training 3

HyperTransport3.0

1/4

0x1F0

Training 3 ff 3ff

14- 84 Training 3

--	--	--

31:0 T3 time

32



HyperTransport 3.0:

PHY_LINK_CLK 100MHz × div_loop /div_refc /phy_div

PLL system clk 33M 30us ~

Ω

3C5000 HT_CORE_CLK 'P L NODE No

L

0x1F4

0x00000000

14- 85

31	Reserved	1	0x0	R/W	
30 26	Soft_phy_hi_div	5	0x0	R/W	PHY No
25	Reserved	1	0x0	R/W	
24 20	Soft_phy_lo_div	5	0x0	R/W	PHY No
19 17	Reserved	3	0x0	R/W	
16 8	Soft_div_loop	9	0x0	R/W	PLL ρ
7 4	Soft_div_refc	4	0x0	R/W	PLL ρ No
3	Locked	1	0x0	R	
2	Bypass ht core	1	0x0	R/W	ǎ L
1	Soft cofig enable	1	0x0	R/W	1 ' b0 1 ' b1
0	Reserved	1	0x0	R/W	

14.5.29 PHY

L PHY γ Ũ γ ǎ

0x1F8

0x00000000

PHY γ L

14- 86 γ L

|--|--|--|--|--|--|

31	Tx_scanin_en	1	0x0	R/W	TX	Y	
30	Rx_scanin_en	1	0x0	R/W	RX	Y	
27:24	Tx_scanin_ncode	4	0x0	R/W	TX	Y	ncode
23:20	Tx_scanin_pcode	4	0x0	R/W	TX	Y	pcode
19:12	Rx_scanin_code	8	0x0	R/W	RX	Y	

14.5.30 PHY

PHY	PHY	$\tilde{\alpha}$	$\tilde{\alpha}$	L		8bit	L
PHY	PHY	$\tilde{\alpha}$	L	L	L	16bit	L
	PHY	$\tilde{\alpha}$	L	L			
	0x1FC						
	0x83308000						
	PHY						

14- 87 PHY

31	Rx_ckpll_term	1	0x1	R/W	PLL [RX
30	Tx_ckpll_term	1	0x0	R/W	PLL [TX
29	Rx_clk_in_sel	1	0x0	R/W	PAD PAD HT1 CLKPAD: 1 ' b0 1 ' b1 PLL
28	Rx_ckdll_sell	1	0x0	R/W	DLL 1 ' b0 PLL 1 ' b1
27:26	Rx_ctle_bitc	2	0x0	R/W	PAD EQD
25:24	Rx_ctle_bitr	2	0x3	R/W	PAD EQD
23:22	Rx_ctle_bitlim	2	0x0	R/W	PAD EQD L
21	Rx_en_ldo	1	0x1	R/W	LDO L 1 ' b0 LDO 1 ' b1 LDO



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Y

31:16	Rx_wait_time	16	0x0	R/W	RX Δ
15:0	Tx_wait_time	16	0x0	R/W	TX Δ

0x248

0x00000000

LDT 2

14- 90 LDT 2

31:30	Reserved	16	0x0	R/W	
29:0	rx lane ts 0	16	0x0	R/W	

0x24C

0x00000000

LDT 3

14- 91 LDT 3

31:30	Reserved	16	0x0	R/W	
29:0	rx lane ts 1	16	0x0	R/W	

0x250

0x00000000

LDT 4

14- 92 LDT 4

31:30	Reserved	16	0x0	R/W	
29:0	rx lane ts 2	16	0x0	R/W	

0x254

0x00000000

LDT 5



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Y

14- 93 LDT

5

31:22	Reserved	10	0x0	R/W	
21:18	wait ctl	4	0x0	R/W	
17:0	phase lock	18	0x0	%IJ	



					o ID MASK
15:0	HT TX POST ID1 BASE	16	0x0	R/W	AXI ID POST o ID BASE

0x268

0x00000000

HT TX POST ID WIN2

14- 97 HT TX POST ID WIN2

31:16	HT TX POST ID2 MASK	16	0x0	R/W	AXI ID POST o ID MASK
15:0	HT TX POST ID2 BASE	16	0x0	R/W	AXI ID POST o ID BASE

0x26C

0x00000000

HT TX POST ID WIN3

14- 98 HT TX POST ID WIN3

31:16	HT TX POST ID3 MASK	16	0x0	R/W	AXI ID POST o ID MASK
15:0	HT TX POST ID3 BASE	16	0x0	R/W	AXI ID POST o ID BASE



14.5.36 Bist

HT bist

0x340

0x00000010

bist L

14- 102 bist L





14.5.37 LDO

PHY ρ LDO

0x350

0xBF A38783

LDO

14- 105 LDO





14.5.40 Unitid

id HT 0 unitid
0x360
0x00000000
unitid L 0
14- 108 unitid L 0

31:21	Reserved	11	0x0	R/W	
23:16	unit_id0	5	0x0	R/W	0~ ° unitid
15:8	axi2unitid0_mask	8	0x0	R/W	0~ ° id
7:0	axi2unitid0_base	8	0x0	R/W	0~ ° id



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Y

7:0	axi2unitid2_base	8	0x0	R/W	2 ⁸ - 0	id
-----	------------------	---	-----	-----	--------------------	----

0x36C

0x00000000

unitid L 3

14- 111 unitid L 3

--	--	--	--	--	--

31:21	Reserved	11	0x0	R/W	
23:16	unit_id3	5	0x0	R/W	3 ⁵ - 0 unitid
15:8	axi2unitid3_mask	8	0x0	R/W	3 ⁸ - 0 id
7:0	axi2unitid3_base	8	0x0	R/W	3 d " 0 " 0 "

J



19:15	LC_VTH1_CTRL_N	5	0x18	R/W	
14:10	LC_VTH1_CTRL_P	5	0x18	R/W	
9:5	LC_VTH2_CTRL_N	5	0x18	R/W	
4:0	LC_VTH2_CTRL_P	5	0x18	R/W	

14.5.44 PLL

PLL ĭ ĭ

0x37C

0x0000600f

PLL

14- 115 PLL





HT [POST
 NONPOST L = ì ò
 0x1C0[17:16] ì
 ì 0 3

0x380

0x00000000

HT 0 0

14- 116 HT 0 0

31	ht_rx_prior0_en	1	0x0	R/W	HT	0 ~
30	ht_rx_prior0_post_en	1	0x0	R/W	HT	0 POST
29	ht_rx_prior0_nonpost_en	1	0x0	R/W	HT	0 NONPOST
1:0	ht_rx_prior0	2	0x0	R/W	HT	0

0x384

0x00000000

HT 0 0

14- 117 HT 0 0

31:16	ht_rx_prior0_base[39:24]	16	0x0	R/W	HT	0 [39:24]
15:0	ht_rx_prior0_mask[39:24]	16	0x0	R/W	HT	0 [39:24]

0x1B8

0x00000000

HT 0 1

14- 118 HT 0 1

31	ht_rx_prior1_en	1	0x0	R/W	HT	1 ~
30	ht_rx_prior1_post_en	1	0x0	R/W	HT	1 POST
29	ht_rx_prior1_nonpost_en	1	0x0	R/W	HT	1 NONPOST
1:0	ht_rx_prior1	2	0x0	R/W	HT	1



0x1BC

0x00000000

HT o 1

14- 119 HT o 1

31:16	ht_rx_prior1_base[39:24]	16	0x0	R/W	HT	o 1	[39:24]
15:0	ht_rx_prior1_mask[39:24]	16	0x0	R/W	HT	o 1	[39:24]

14.5.46

o 14.5.10

o HT [0xFD_0xxx_xxxx

o ~ L

0x3C0

0x00000000

HT o 0

14- 120 HT o 0

31	ht_rx_ir0_en	1	0x0	R/W	HT	o 0	~

0x3C4

0x00000000

HT o 0

14- 121 HT o 0

31:16	ht_rx_ir0_base[39:24]	16	0x0	R/W	HT	o	[39:24]
15:0	ht_rx_ir0_mask[39:24]	16	0x0	R/W	HT	o	[39:24]

14.6 HyperTransport

HyperTransport o v PCI v



3A6000

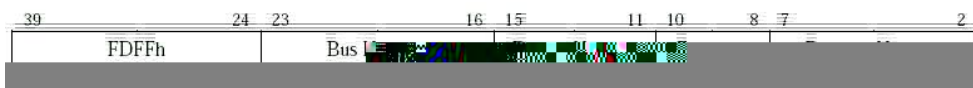
Y

√ 7 i 14- 6 ↓ 7 HT
0xFD_FE00_0000 0xFD_FFFF_FFFF HT √ 3A6000

Type 0:



Type 1:



15.1 UART

UART 是 L 的 1 个外设，它支持 16 字节的 FIFO。UART 的寄存器地址如下表所示。

寄存器名称	地址	大小	复位值
UART0 寄存器	0x1FE001E0	4 字节	0
UART1 寄存器	0x1FE001E8	4 字节	0

UART 的寄存器地址如下表所示。

寄存器名称	地址	大小	复位值
UART0 寄存器	0x1FE001E0	4 字节	0
UART1 寄存器	0x1FE001E8	4 字节	0

UART 的寄存器地址如下表所示。

寄存器名称	地址	大小	复位值
UART0 寄存器	0x1FE001E0	4 字节	0
UART1 寄存器	0x1FE001E8	4 字节	0

UART 的寄存器地址如下表所示。

寄存器名称	地址	大小	复位值
UART0 寄存器	0x1FE001E0	4 字节	0
UART1 寄存器	0x1FE001E8	4 字节	0

15.1.1 寄存器定义



15.1.2 IER

[7 0]

0x01

0x00

7:4	Reserved	4	RW	
3	IME	1	RW	Modem '0' - '1' -
2	ILE	1	RW	'0' - '1' -
1	ITxE	1	RW	'0' - '1' -
0	IRxE	1	RW	'0' - '1' -

15.1.3 IIR

[7 0]

0x02

0xc1

7:4	Reserved	4	R	
3:1	II	3	R	
0	INTp	1	R	

L_w

Bit 3	Bit 2	Bit 1				L
0	1	1	1st		≠	LSR
0	1	0	2nd	∩	FIFO trigger	FIFO trigger



3A6000

Y

1	1	0	2nd		FIFO		FIFO
					4	$\dot{\rho}$	
						Ω	
0	0	1	3rd			Ω	[THR
							IIR
0	0	0	4th	Modem			



				' 0 ' –
5	spb	1	RW	' 0 ' – ' 1 ' – LCR[4] 1 † 0 LCR[4] 0 † 1
4	eps	1	RW	' 0 ' – 1 ' ' 1 ' – 1
3	pe	1	RW	' 0 ' – ' 1 ' – † ∞
2	sb	1	RW	' 0 ' – 1 ' 1 ' – 5 1.5 † 2
1:0	bec	2	RW	' 00 ' – 5 ' 01 ' – 6 ' 10 ' – 7 ' 11 ' – 8

15.1.6 MODEM

MCR

Modem L

[7 0]

0x04

0x00



7:5	Reserved	3	W
4	Loop	1	W L

' 0 ' –

' 1 ' –



				DTR : DSR RTS : CTS Out1 : RI Out2 : DCD
3	OUT2	1	W	DCD
2	OUT1	1	W	RI
1	RTSC	1	W	RTS ~ L
0	DTRC	1	W	DTR ~ L

15.1.7

LSR

[7 0]

0x05

0x00

7	ERROR	1	R	
				‘ 1 ’ –
				‘ 0 ’ –
6	TE	1	R	
				‘ 1 ’ – FIFO 0



3	FE	1	R	' 1 ' – ' 0 ' –
2	PE	1	R	' 1 ' – 11 ' 0 ' –
1	OE	1	R	11 ' 1 ' – 11 ' 0 ' – 11
0	DR	1	R	' 0 ' – FIFO ' 1 ' – FIFO

LSR[0] ↓ FIFO ∞ LSR[4:1] LSR[7] LSR[6:5] FIFO Ω

15.1.8 MODE8



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15.1.9 FIFO RFC

FIFO

[7 0]

0x08

0x00



7:0

RFC

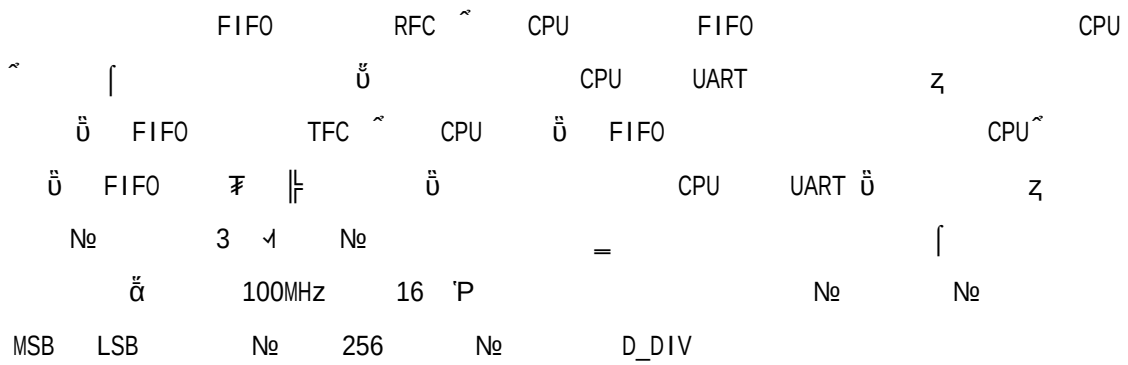
3

0x02

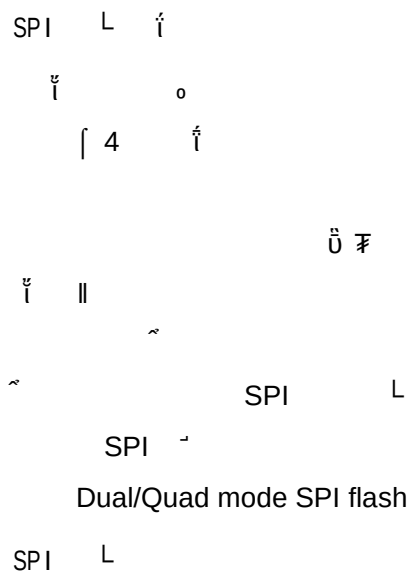
0x00

7:0	D_DIV	8	RW	No	No
-----	-------	---	----	----	----

15.1.12



15.2 SPI



15- 1 SPI L No

SPI Boot	0x1C00_0000-0x1CFF_FFFF	16MByte
SPI Memory	0x1D00_0000-0x1DFF_FFFF	16MByte
SPI Register	0x1FE0_01F0-0x1FE0_01FF	16Byte



SPI Boot
SPI Memory CPU

15.2.1 SPCR

L
[7 0]
0x00
0x10

7	Spie	1	RW	0 1
6	spe	1	RW	0 1
5	Reserved	1	RW	
4	mstr	1	RW	master 1
3	cpol	1	RW	
2	cpha	1	RW	1 0 0 1
1:0	spr	2	RW	sc lk_o Ne sper spre

15.2.2 SPSR

[7 0]
0x01
0x05

7	spif	1	RW	1 0 1 1
6	wcol	1	RW	0 1 1 1 1 1
5:4	Reserved	2	RW	
3	wffull	1	RW	0 1
2	wfempty	1	RW	0 1
1	rffull	1	RW	1
0	rfempty	1	RW	1



15.2.3

TxFIFO

[7 0]

0x02

0x00

7:0	Tx FIFO	8	W	
-----	---------	---	---	--

15.2.4

SPER

[7 0]

0x03

0x00

7:6	icnt	2	RW	00 - 101 - 211 - 3
5:2	Reserved	4	RW	
1:0	spre	2	RW	SprNo

No

spre	00	00	00	00	01	01	01	01	10	10	10	10
spr	00	01	10	11	00	01	10	11	00	01	10	11
No	2	4	16	32	8	64	128	256	512	1024	2048	4096

15.2.5

SFC_PARAM

SPI Flash 0 L

[7 0]

0x04

0x21



7:4	clk_div	4	RW	No No {spre,spr} _v
3	dual_io	1	RW	I I/O
2	fast_read	1	RW	
1	burst_en	1	RW	spi flash
0	memory_en	1	RW	spi flash csn[0]~ L

15.2.6

SFC_SOFTCS

SPI Flash L
S c L

0



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Ô





15.2.11

1 BUF1

SPI Flash

1

[7 0]

0x0b

0x00



0x0e

0x00

7:0	time2	8	RW	8
-----	-------	---	----	---

15.2.15 SPI

quad_io SPI L (dual mode) quad mode

SPI flash dual_io SPI L

quad_io SPI L BIOS

L

SPI FLASH

(dummy clocks) SPI L FLASH

(0x8-0xe) CMD 0x9 SPI FLASH

1. CMD 0x9 SPI FLASH

2. SPI FLASH

TIMER0-TIMER2(0xc-0xe)

3. SPI FLASH

BUF0-BUF1(0xa-0xb) SPI FLASH

4. CTRL[7:1] CTRL[1](nbmode)

CTRL[7:4](nbyte)

5. CTRL[0]

FLASH

15.3 I2C



$\dot{p}$ $\textcircled{P}$ $\ddot{u}$ $\dot{p}$
 SLV_CTRL[6:0]
 I2C0 L 0x1FE00120
 I2C1 L 0x1FE00130
 $\dot{i}$ $\dot{p}$

15.3.1

PRERlo

N_0
 [7 0]
 0x00
 0xff

7:0	PRERlo	8	RW	N_0	8

15.3.2

PRERhi

N_0
 [7 0]
 0x01
 0xff

7:0	PRERhi	8	RW	N_0	8

N_0 prescale LPB PCLK clock_aSCL
 $\frac{1}{f}$ clock_s ↑ τ
 $\text{Prcescale} = \text{clock_a}/(4*\text{clock_s})-1$

15.3.3

CTR

L
 [7 0]
 0x02
 0x20

--	--	--	--	--	--



7	EN	1	RW	1 0 No
6	IEN	1	RW	1 t
5	MST_EN	1	RW	0 slave 1 master
4:0	Reserved	5	RW	

15.3.4

TXR

0

[7 0]

0x03

0x00

7:1	DATA	7	W	0
0	DRW	1	W	Ω

15.3.5

RXR

[7 0]

0x03

0x00

7:0	RXR	8	R	└
-----	-----	---	---	---

15.3.6

CR

[7 0]



0x04

0x00

7	STA	1	W	START
6	STO	1	W	STOP
5	RD	1	W	
4	WR	1	W	
3	ACK	1	W	
2:1	Reserved	2	W	
0	IACK	1	W	

I2C

'0' bit 3 1

L ack i ack

15.3.7

SR

[7 0]

0x04

0x00

7	RxACK	1	R	
6	Busy	1	R	I2C
5	AL	1	R	I2C I2C L 1
4:2	Reserved	3	R	
1	TIP	1	R	
0	IF	1	R	



15.3.8 SLV_CTRL

L

[7 0]

0x07

0x00

7	SLV_EN	1	WR	MST_EN 0 ~
6 0	SLV_ADDR	7	WR	I2C ~

15.4 AVS

AVS L

0x1FE00160

15- 2 AVS L No

AVS Register	0x1FE0_0160-0x1FE0_016F	16B

15.4.1 CSR

L

[31 0]

0x0

0x0

31	resyn	1	RW	1 0 1 0
30:29	mask_ack	2	RW	0 1 mask alert_ack
28	mask_i	1	RW	1 mask alert_i
27	mask_s	1	RW	1 mask alert_s
26	mask_c	1	RW	1 mask alert_c
25	mask_a	1	RW	1 mask alert_a
24	rx_ctrl	1	RW	L 1 AVS 0 AVS



				0
23:20	rx_delay	4	RW	1 1 2 1 0
19:17	clk_div	3	RW	No 0x0 No 0x1 No 0x2 No 0x3 M'E No 0x4 M No 0x5 'E M No No
16	Dmux	1	RW	1 1 0 1 0
15:0	reserved	16	—	—

15.4.2

Mreg

L

[31 0]

0x4

0x0

31	TX_EN	1	RW	Ω 1 AVS
30:29	cmd	2	RW	0x0 Ω 0x1 Ω 1 0x2 0x3 Ω cmd 0
28	group	1	RW	0 AVS 1 ≠ 1 L 1
27:24	cmd_type	4	RW	0x0 1 1LSB=1mv 0x1 1 cmd_data 0x2 0x3 0x4 1 Ω 0x5 w 0x6~0xd 0xe 0xf
23:20	rail_sel	4	RW	1 0xf 1
19:4	cmd_data	16	RW	Ω 1 0 1
3:0	reserved			

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